AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1. (Previously Presented) A multi-layered lithography structure, the structure comprising:
a substrate;
a first resist layer with a first surface coupled to said substrate, said first resist layer having a first resist latent image area;
an opaque barrier layer on a second surface of said first resist, said opaque barrier layer covering said first resist latent image area;
a second resist layer coupled to said opaque barrier layer, said second resist layer having a second resist latent image area; and
a means for developing said multi-layered lithography structure wherein said first resist layer is exposed prior to depositing said opaque barrier layer, wherein said first resist latent image area is developed subsequent to said second resist latent image area, and wherein a barrier layer developed area is removed prior to developing said first resist latent image area.

Claim 2. (Previously Presented) The structure of claim 1, further comprising a second opaque barrier layer on said second resist layer, and a third resist layer on said second opaque barrier layer with a third resist latent image area, wherein said second resist latent image area is developed subsequent to said third resist latent image area, and wherein a second barrier layer developed area is removed prior to developing said second resist latent image area.

Claim 3. (Previously Presented) The structure of claim 1, wherein said first resist latent image area, said barrier layer developed area, and said second resist latent image area have variable patterns.

Claim 4. (Original) The structure of claim 1, further comprising a plurality of said structures on said substrate.

Claim 5. (Previously Presented) The structure of claim 1, wherein said first resist latent image area, said barrier layer developed area, and said second resist latent image area have variable sizes.

Claim 6. (Previously Presented) The structure of claim 1, wherein said opaque barrier layer is an opaque metallic layer.

Claim 7. (Previously Presented) The structure of claim 1, wherein said first resist layer and said second resist layer are selected from at least one of the group consisting of: azide, polymers and copolymers of polymethylmethacrylate (PMMA), and an epoxy novolac.

Claim 8. (Original) The structure of claim 1 wherein said substrate is selected from at least one of the group consisting of: silicon, gallium arsenide, germanium, glass, and metal.

Claim 9. (Previously Presented) A method of fabricating a multi-layer lithographic semiconductor, comprising:
applying a first resist layer to a semiconductor substrate;
masking said first resist layer and exposing said first resist layer, thereby forming a first latent image in said first resist layer;
adding an opaque barrier layer to said first resist layer covering said first latent image;
applying a second resist layer to said opaque barrier layer;
masking said second resist layer and exposing said second resist layer, thereby forming a second latent image in said second resist layer;
removing said second latent image;

etching said opaque barrier layer; and
removing said first latent image.

Claim 10. (Original) The method of claim 9, further comprising preparing said substrate.

Claim 11. (Original) The method of claim 9, further comprising applying post-application resist treatments.

Claim 12. (Original) The method of claim 11, wherein said post-application resist treatments are selected from at least one of the group consisting of: softbake, hydration, and ammonia based image reversal.

Claim 13. (Original) The method of claim 9, wherein a shape of said first latent image and the second latent image is selected from the group consisting of: square, rectangle, triangle, circle, oval, and polygon.

Claim 14. (Original) The method of claim 9, wherein said etching is selected from the group consisting of wet etch, dry etch and develop/exposure.

Claim 15. (Original) The method of claim 9, wherein said exposing uses rays selected from at least one of the group consisting of ultraviolet light, electrons, and x-rays.

Claim 16. (Original) The method of claim 9, further comprising using alignment tools.

Claim 17. (Previously Presented) The method of claim 9, further comprising adding a second opaque barrier layer on said second resist layer, applying a third resist layer on said second opaque barrier layer,

masking said third resist layer and exposing said third resist layer, thereby forming a third latent image in said third resist layer, removing said third latent image, etching said second opaque barrier layer, and removing said second latent image.

Claim 18. (Previously Presented) A lithographic process for fabricating multi-layer semiconductor devices, comprising:
providing a substrate;
coating a first resist layer onto said substrate;
exposing said first resist layer with a mask to form a first layer exposed area and a first layer unexposed area;
depositing an opaque barrier layer on said first layer exposed area and said first layer unexposed area;
coating a second resist layer onto said opaque barrier layer;
exposing said second resist layer with a mask to form a second layer exposed area and a second layer unexposed area;
developing said second layer exposed area;
etching said opaque barrier layer;
developing said first layer exposed area; and
fabricating devices on said substrate.

Claim 19. (Original) The lithographic process according to claim 18, wherein said depositing is selected from the group consisting of: thermal evaporation, spin coating, spray coating, and electroless plating.

Claim 20. (Original) The lithographic process according to claim 18, wherein said step of coating is spun coating.